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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,883	02/20/2004	David James Seal	550-509	4228

23117 7590 10/16/2006

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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,883	SEAL ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 have been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-17, 19-28, and 30-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Jagger (GB 2,289,354).

4. As per Claim 1, Jagger teaches: Apparatus for processing data, said apparatus comprising:

data processing logic operable to perform data processing operations (Page 4, Lines 17-18, the processor core); and

an instruction decoder operable to decode program instructions specifying data processing operations to be performed by said data processing logic and to control said data processing logic to perform said data processing operations (Page 4, Lines 19-21, the decoding means); wherein

said instruction decoder is operable in a first mode in which program instructions of a first instruction set are decoded (Page 7, Lines 25-28) and in a second mode in which program instructions of a second instruction set are decoded (Page 7, Lines 25-

31), a subset of program instructions of said first instruction set having a common storage order compensated encoding with a subset of program instructions of said second instruction set and forming a common subset of instructions representing at least one class of instructions (Page 4, Lines 24-29), said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode (Page 8, Lines 19-27. The one to one mapping of instructions means that the instructions will be decoded the same way, meaning the data will be processed the same way regardless of which way it was fetched or decoded, for those instructions).

5. As per Claim 2, Jagger teaches: Apparatus as claimed in claim 1, wherein said instruction decoder is operable to use common portions of said data processing logic to execute instructions of said common subset of instructions (Page 3, Line 33 – Page 4, Line 1. Registers are shared between the instruction sets).

6. As per Claim 3, Jagger teaches: Apparatus as claimed in claim 1, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using coprocessor logic common to said first instruction set and said second instruction set (Page 3, Line 33 – Page 4, Line 1. Registers are shared between the instruction sets).

7. As per Claim 4, Jagger teaches: Apparatus as claimed in claim 3, wherein all unconditional coprocessor instructions are within said common subset (Page 9, Lines 31-36, the smaller bit size instructions (the subset) are unconditional).

8. As per Claim 5, Jagger teaches: Apparatus as claimed in claim 1, wherein said first instruction set is a fixed length instruction set of N-bit instructions (Page 6, Lines 17-25, where N equals 16).

9. As per Claim 6, Jagger teaches: Apparatus as claimed in claim 5, wherein N is one of 32 or 16 (Page 6, Lines 17-25, where N equals 16).

10. As per Claim 8, Jagger teaches: Apparatus as claimed in claim 1, wherein at least one program instruction within said common subset of instructions performs common data processing operations in either said first mode or said second mode but generates different result data values depending upon whether said instruction decoder is operating in said first mode or said second mode (Page 6, Lines 12-14, the PC is updated differently in the different modes).

11. As per Claim 9, Jagger teaches: Apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand (Page 6, Lines 7-8).

12. As per Claim 10, Jagger teaches: Apparatus as claimed in claim 9, wherein a different relationship is maintained between said program counter value and an address of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode (Page 6, Lines 12-14).

13. As per Claim 11, Jagger teaches: Apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand (Page 5 Line 31 – Page 6 Line 7).

14. As per Claim 12, Jagger teaches: A method of processing data, said method comprising the steps of:

performing data processing operations with data processing logic (Page 4, Lines 17-18, the processor core); and

decoding with an instruction decoder program instructions specifying data processing operations to be performed by said data processing logic and controlling said data processing logic to perform said data processing operations (Page 4, Lines 19-21, the decoding means); wherein

in a first mode program instructions of a first instruction set are decoded (Page 7, Lines 25-28) and in a second mode program instructions of a second instruction set are decoded (Page 7, Lines 25-31), a subset of program instructions of said first instruction set having a common storage order compensated encoding with a subset of program instructions of said second instruction set and forming a common subset of instructions

representing at least one class of instructions (Page 4, Lines 24-29), said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode (Page 8, Lines 19-27. The one to one mapping of instructions means that the instructions will be decoded the same way, meaning the data will be processed the same way regardless of which way it was fetched or decoded, for those instructions).

15. As per Claim 13, Jagger teaches: A method as claimed in claim 12, wherein common portions of said data processing logic are used to execute instructions of said common subset of instructions (Page 3, Line 33 – Page 4, Line 1. Registers are shared between the instruction sets).

16. As per Claim 14, Jagger teaches: A method as claimed in claim 12, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using coprocessor logic common to said first instruction set and said second instruction set (Page 3, Line 33 – Page 4, Line 1. Registers are shared between the instruction sets).

17. As per Claim 15, Jagger teaches: A method as claimed in claim 14, wherein all unconditional coprocessor instructions are within said common subset (Page 9, Lines

31-36, the smaller bit size instructions (the subset) are unconditional).

18. As per Claim 16, Jagger teaches: A method as claimed in claim 12, wherein said first instruction set is a fixed length instruction set of N-bit instructions (Page 6, Lines 17-25, where N equals 16).

19. As per Claim 17, Jagger teaches: A method as claimed in claim 16, wherein N is one of 32 or 16 (Page 6, Lines 17-25, where N equals 16).

20. As per Claim 19, Jagger teaches: A method as claimed in claim 12, wherein at least one program instruction within said common subset of instructions performs common data processing operations in either said first mode or said second mode but generates different result data values depending upon whether said instruction decoder is operating in said first mode or said second mode (Page 6, Lines 12-14, the PC is updated differently in the different modes).

21. As per Claim 20, Jagger teaches: A method as claimed in claim 19, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand (Page 6, Lines 7-8).

22. As per Claim 21, Jagger teaches: A method as claimed in claim 20, wherein a different relationship is maintained between said program counter value and an address

of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode (Page 6, Lines 12-14).

23. As per Claim 22, Jagger teaches: A method as claimed in claim 19, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand (Page 5 Line 31 – Page 6 Line 7).

24. As per Claim 23, Jagger teaches: A computer program product having a computer program operable to control a data processing apparatus containing data processing logic operable to perform data processing operations (Page 4, Lines 17-18, the processor core), said computer program comprising:

program instructions of a first instruction set (Page 7, Lines 25-28) and program instructions of a second instruction set (Page 7, Lines 25-31), that control said data processing logic to perform said data processing operations; wherein

a subset of program instructions of said first instruction set have a common storage order compensated encoding with a subset of program instructions of said second instruction set and form a common subset of instructions representing at least one class of instructions (Page 4, Lines 24-29), said common subset of instructions controlling data processing logic to perform the same data processing operations independent of whether instructions of said first instruction set or of said second instruction set are being decoded (Page 8, Lines 19-27. The one to one mapping of instructions means that the instructions will be decoded the same way, meaning the

data will be processed the same way regardless of which way it was fetched or decoded, for those instructions).

25. As per Claim 24, Jagger teaches: A computer program product as claimed in claim 23, wherein common portions of said data processing logic are used to execute instructions of said common subset of instructions (Page 3, Line 33 – Page 4, Line 1. Registers are shared between the instruction sets).

26. As per Claim 25, Jagger teaches: A computer program product as claimed in claim 23, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using coprocessor logic common to said first instruction set and said second instruction set (Page 3, Line 33 – Page 4, Line 1. Registers are shared between the instruction sets).

27. As per Claim 26, Jagger teaches: A computer program product as claimed in claim 25, wherein all unconditional coprocessor instructions are within said common subset (Page 9, Lines 31-36, the smaller bit size instructions (the subset) are unconditional).

28. As per Claim 27, Jagger teaches: A computer program product as claimed in claim 23, wherein said first instruction set is a fixed length instruction set of N-bit

instructions (Page 6, Lines 17-25, where N equals 16).

29. As per Claim 28, Jagger teaches: A computer program product as claimed in claim 27, wherein N is one of 32 or 16 (Page 6, Lines 17-25, where N equals 16).

30. As per Claim 30, Jagger teaches: A computer program product as claimed in claim 23, wherein at least one program instruction within said common subset of instructions performs common data processing operations when instructions of either said first instruction set or said second instruction set are being decoded but generates different result data values (Page 6, Lines 12-14, the PC is updated differently in the different modes).

31. As per Claim 31, Jagger teaches: A computer program product as claimed in claim 30, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand (Page 6, Lines 7-8).

32. As per Claim 32, Jagger teaches: A computer program product as claimed in claim 31, wherein a different relationship is maintained between said program counter value and an address of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode (Page 6, Lines 12-14).

33. As per Claim 33, Jagger teaches: A computer program product as claimed in claim 30, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand (Page 5 Line 31 – Page 6 Line 7).

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 7, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagger, in view of McFarland et al. (USPN 5,781,753, herein McFarland).

36. As per Claim 7, Jagger teaches an Apparatus as claimed in claim 1, but fails to explicitly teach:

wherein said second instruction set is a variable length instruction set.

Jagger teaches a system to allow a first and second instruction set to run on the same processor without a large amount of increased logic, but does not explicitly teach that the second instruction set is a variable length instruction set. However, McFarland teaches that the x86 architecture, one of the most widely used architectures in PC's, and what made PCs into a mass-market item (Column 2, Lines 9-20), contains variable-length instructions that need to be dealt with when designing a machine to run the

architecture (Column 5, Lines 56-65). Given the popularity and wide usage of the x86 processor, and the advantage of using Jagger's system to allow instruction sets of different lengths to work together with minimal cost, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Jagger's invention into a machine running an x86 architecture, which would make variable-length instructions one of the instruction sets Jagger deals with. Claims 18 and 29 have similar limitations and are rejected for the same reasons.

Response to Arguments

37. Applicant's arguments filed 8/1/2006 have been fully considered but they are not persuasive.

Applicant has essentially argued that Jagger fails to teach the claim limitation of "a subset of program instructions of said first instruction set having a common storage order compensated encoding with a subset of program instructions of said second instruction set and forming a common subset of instructions representing at least one class of instructions". Applicant has argued that due the Jagger mapping one instruction set to another, he cannot anticipate the aforementioned claim language. However, the term "common storage order compensated encoding" is an extremely broad limitation with no concrete definition in the specification, and was interpreted in the broadest reasonable sense, that the two instruction sets had a common storage ordering. While the cited portions of the reference were primarily used to point out to the Applicant that the instruction sets are subsets of each other, it can further be seen in Figures 5-6,

which show that both instruction sets are stored in the same Endian format, thus a "common storage order compensated encoding". In addition, "common" is not specific enough to overcome the teachings of Jagger, as a "common encoding" could be interpreted as the two sets having even just one bit in common with the other, there is no degree to which they are similar or dissimilar in the claim language, and a conversion could still be required between "common encodings", depending upon the degree of commonality which has not been established, thus the similarities in stored bits between the sets disclosed by Jagger are further a "common encoding".

Applicant has further argued Claim 3, stating that "sharing registers between instruction sets in no way means or suggests that a class of instructions is shared". Claim 3 states that common logic can be used by a class of instructions to control the processor, and Examiner pointed out that registers are shared logic, thus this argument appears moot, as Examiner did not make the assumption implied by the Applicant, but rather pointed out that a register is logic and is common to both instruction sets.

Conclusion

38. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
Art Unit 2183

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